ICP2 Family Programmers

Programming Times

###	*Device*	*Time,sec*	*Flash Memory, bytes*	*EEPROM, bytes*	*Operations*	*Conditions*
1.	PIC10F200	0.95	510	-	Erase + Program + Verify	PGC≈320KHz, VddOff=20ms
2.	PIC12F508	1.7	1022	-	Erase + Program + Verify	PGC≈320KHz, VddOff=20ms
3.	PIC16F631	1.5	2048	excluded	Erase + Program + Verify	PGC≈320KHz, VddOff=20ms
		2.5	2048	128	Erase + Program + Verify	PGC≈320KHz, VddOff=20ms
4.	PIC16F716	2.0	4096	-	Erase + Program + Verify	PGC≈320KHz, VddOff=20ms
5.	PIC16F73	3.8	8192	-	Erase + Program + Verify	PGC≈320KHz, VddOff=20ms
6.	PIC16F874A	2.5	8192	excluded	Erase + Program + Verify	PGC≈320KHz, VddOff=20ms
		3.9	8192	128	Erase + Program + Verify	PGC≈320KHz, VddOff=20ms
7.	PIC16F76	8.2	16,384	-	Erase + Program + Verify	PGC≈320KHz
8.	PIC16F887	6.7	16,384	excluded	Erase + Program + Verify	PGC≈320KHz
		9.4	16,384	256	Erase + Program + Verify	PGC≈320KHz
9.	PIC16F917	6.8	16,384	excluded	Erase + Program + Verify	PGC≈320KHz
		9.4	16,384	256	Erase + Program + Verify	PGC≈320KHz

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ICP2 Family: Programming Times

###	*Device*	*Time,sec*	*Flash Memory, bytes*	*EEPROM, bytes*	*Operations*	*Conditions*
10.	PIC18F4520	4.5	32,768	excluded	Erase + Program + Verify	PGC=2.5MHz
		5.6	32,768	256	Erase + Program + Verify	PGC=2.5MHz
11.	PIC18F8722	12.0	131,072	excluded	Erase + Program + Verify	PGC=2.5MHz
		16.5	131,072	1,024	Erase + Program + Verify	PGC=2.5MHz
12.	PIC24FJ128GA008	27.2	132,090	-	Erase + Program + Verify	PGC=2.5MHz
13.	dsPIC30F2010	2.7	12,288	excluded	Erase + Program + Verify	PGC=2.5MHz, VddOff=20ms
		3.2	12,288	1,024	Erase + Program + Verify	PGC=2.5MHz, VddOff=20ms
14.	dsPIC30F6014	31.8	147,456	excluded	Erase + Program + Verify	PGC=2.5MHz
		33.2	147,456	4,096	Erase + Program + Verify	PGC=2.5MHz
15.	dsPIC33FJ128GP708	27.4	132,096	-	Erase + Program + Verify	PGC=2.5MHz

Notes:
1. VddOff defines a delay between power OFF and power ON which allows discharging Vdd capacitor on a target board. Default VddOff delay is about 170 ms
2. Programming times are measured on ICP2 programmer in the following conditions:
   - standalone mode
   - hardware activation of programming (GO button)
   - DLL version 4.4.2 with firmware version 11.4 (July-2007)
3. All results are also applicable to ICP2-GANG since ICP2 and ICP2-GANG use the same internal programmer module(s)
4. Programming times depend on implemented programming algorithms. Softlog Systems reserves the right to change programming algorithms at any time without notice